SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor integrated circuit devices such as LSI, particularly to a semiconductor integrated circuit device which inhibits a capability of a circuit from being degraded by a power voltage drop generated in the circuit disposed in the semiconductor integrated circuit device.

This application is counterpart of Japanese patent application, Serial Number 382455/2003, filed November 12, 2003, the subject matter of which is incorporated herein by reference.

Description of the Related Art

In recent years, semiconductor integrated circuit devices such as LSI have been requested to have an enlarged scale or multiple functions, and there has been a tendency to complication of a constitution of the semiconductor integrated circuit device and to an increase of a circuit area. This has involved an increase in a resistance by drawing around a power wiring and a ground wiring disposed in the semiconductor integrated circuit device, or in a decrease in a power voltage for the purpose of saving a power consumption and increasing a speed of the circuit. This has caused a voltage drop of a supply voltage in the circuit disposed in a position distant from a power supply,

and has caused problems such as a defective operation and an operation speed decrease of the circuit.

To solve the problems, a method has been used in which supply portions of the power voltage are increased or the supply portions are devised to decrease circuits to be disposed in positions distant from the supply portions or a meshed or thick power wiring is disposed to reduce an effective wiring resistance.

Moreover, as a device which inhibits the voltage drop of the supply voltage in a general circuit disposed in the position distant from the power supply, a semiconductor integrated circuit device has been known which detects an internal power voltage level and an internal ground voltage level of the general circuit disposed in a semiconductor integrated circuit. In the device, the general circuit is controlled so as to compensate for a change of the voltage level of the general circuit by obtained internal power voltage detection signal and internal ground voltage detection signal (e.g., see Japanese Patent Application Laid-Open No.05-315544).

However, in the method of increasing the power supply portions, input pads need to be increased in order to secure the power supply portions. In the method of devising the shape of the power wiring or thickening the power wiring, there is a problem that a layout area of a power wiring portion increases. In this method, the effective resistance of the power wiring decreases but is

not completely eliminated. Therefore, this method cannot sufficiently cope with the reduced voltage or the enlarged scale, and cannot be said to be an actually useful method.

Moreover, the conventional semiconductor integrated circuit device for inhibiting the voltage drop of the supply voltage in the general circuit disposed in the position distant from the power supply has a problem that a circuit for detecting the internal power voltage level and internal ground voltage level is required for each general circuit. Another problem is that the wiring on the semiconductor integrated circuit device is complicated.

SUMMARY OF THE INVENTION

The present invention has been developed to solve the above-described problem, and an object thereof is to provide a semiconductor integrated circuit device capable of eliminating an influence of a power voltage drop generated in a circuit disposed in the semiconductor integrated circuit device to inhibit an operation defect or an operation speed decrease of the circuit.

To achieve the above-described object, according to the present invention, there is provided a first semiconductor integrated circuit device comprising: a power wiring whose one end is connected to a power supply; a ground wiring whose one end is connected to a ground; and a plurality of circuits connected in parallel between the

power wiring and the ground wiring. The other end of the ground wiring is connected to a current generating section for generating a predetermined current in a state in which the section is connected to a negative power supply.

That is, the ground wiring of the first semiconductor integrated circuit device is connected to the current generating section. The current generating section generates the predetermined current in the state in which the section is connected to the negative power supply.

Accordingly, a direction of the current flowing through the ground wiring corresponds to that extending to a ground from the negative power supply (current generating section). Potentials in nodes which are points connecting a plurality of circuits to the ground wiring become higher, when the nodes are closer to the ground. On the other hand, the potential in the node closer to the power supply becomes higher even on a power wiring side. Therefore, a potential difference between the power supply and the ground can be secured to hold a sufficient voltage level in each circuit, and the operation defect or the operation speed decrease of the circuit can be inhibited.

According to the present invention, there is provided a second semiconductor integrated circuit device comprising: a power wiring whose one end is connected to a power supply; a ground wiring whose one end is connected to a ground; a plurality of circuits connected in parallel between the power wiring and the ground wiring; and a

current generating section whose one end is connected to the other end of the ground wiring to generate a predetermined current in a state in which the other end of the section is connected to a negative power supply.

That is, in the second semiconductor integrated circuit device, the current generating section is disposed in the semiconductor integrated circuit device.

According to the present invention, there is provided a third semiconductor integrated circuit device comprising: a power wiring whose one end is connected to a power supply; a ground wiring whose one end is connected to a ground; a plurality of circuits connected in parallel between the power wiring and the ground wiring; a negative power supply; and a current generating section whose one end is connected to the ground wiring and whose other end is connected to the negative power supply to generate a predetermined current.

That is, in the third semiconductor integrated circuit device, the negative power source and current generating section are disposed in the semiconductor integrated circuit device.

Since the second and third semiconductor integrated circuit devices function in the same manner as in the first semiconductor integrated circuit device of the present invention, the potential difference between the power supply and the ground is secured, the sufficient voltage level can be held in each circuit, and the

operation defect or the operation speed decrease of the circuit can be inhibited.

In the first to third semiconductor integrated circuit devices, the current generating section is preferably disposed in a wiring portion most distant from a portion in which a ground potential of the ground wiring is supplied.

It is to be noted that in the first to third semiconductor integrated circuit devices, the current generating section may be either one of a current source and an operating circuit which consumes a predetermined current to operate. That is, the current generating section may be the current source or the operating circuit which consumes the predetermined current to operate.

For example, the operating circuit which consumes the predetermined current to operate may be a clock generator which outputs a clock signal. Since the clock generator consumes much current, a sufficient voltage level can be held in the plurality of circuits connected in parallel between the power wiring and the ground wiring. The clock generator is preferably connected to a level shifter for converting a level of the outputted clock signal to supply the clock signal to the plurality of circuits.

As described above, according to the present invention, since the ground wiring of the semiconductor integrated circuit device is connected to the current

generating section and negative power supply, an effect is produced that an influence of a power voltage drop generated in the circuit disposed in the semiconductor integrated circuit device is eliminated and an operation defect or operation speed decrease of the circuit can be inhibited.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit constitution diagram of a semiconductor integrated circuit device according to a first embodiment; and

FIG. 2 is a circuit constitution diagram of the semiconductor integrated circuit device according to a second embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

[First Embodiment]

FIG. 1 is a circuit constitution diagram of a semiconductor integrated circuit device according to a first embodiment.

As shown, a power terminal 12, a ground terminal (ground pad) 14, and a negative power terminal 16 are disposed in a semiconductor integrated circuit device 10. The power terminal 12 is connected to an external power

supply, and a power voltage (Vdd) is supplied to the power terminal. The ground terminal 14 is connected to a ground (0 V). An external negative power supply is connected to the negative power terminal 16, and a negative power voltage (-Vdd) is supplied to the terminal. In this case, in the present embodiment, the negative power supply is disposed so that a voltage having the same magnitude as that of the voltage between the power supply and the ground is generated between the negative power supply and the ground.

Moreover, the power terminal 12 is connected to a power wiring 18, and the ground terminal 14 is connected to a ground wiring 20. A plurality of circuits including a first circuit 301 to an f-th circuit 30f are connected in parallel in order from the circuit closest to the power supply and ground between the power wiring 18 and the ground wiring 20.

Furthermore, a current source 22 which is a current generating section is disposed between a node Gf and the negative power terminal 16 on the side of the ground wiring 20 in the f-th circuit 30f disposed in a region most distant from the ground among the plurality of circuits. That is, the current source 22 is disposed in a wiring portion most distant from the ground terminal (ground pad) 14 for supplying a ground potential (0 V) to the ground wiring 20, and generates a current so that a direction of the current flowing through the ground wiring

20 extends toward the negative power supply (current source 22) from the ground.

An operation of the semiconductor integrated circuit device 10 will hereinafter be described.

When a current is supplied from the power wiring 18, the current flows into the ground wiring 20 through the respective circuits 301 to 30f. At this time, when the current flows through each resistance (hereinafter referred to as the power wiring resistance) disposed in the power wiring 18, a voltage drop is generated. Concretely, assuming that the current flowing through a power wiring resistance Rv1 is Iv1, the voltage drop to a node V1 of the first circuit 301 on the power wiring 18 from the power supply is Rv1×Iv1. Assuming that the current flowing through a power wiring resistance Rv2 is Iv2, the voltage drop to a node V2 of the second circuit 302 from the node V1 is Rv2×Iv2. Therefore, the voltage drop to the node V2 from the power supply is Rv1×Iv1+Rv2×Iv2 which is obtained by integrating the respective voltage drops. Similarly, the voltage drop to the node Vf on the power wiring 18 side of the f-th circuit 30f from the power supply indicates a value obtained by integrating all the voltage drops in the respective power wiring resistances.

Therefore, as the respective nodes V1, V2, ... Vf on the power wiring 18 are distant from the power supply, the potentials in the nodes drop.

On the other hand, when the current source 22

connected to the negative power supply is not disposed in the ground wiring 20, the direction of the current flowing through each resistance (hereinafter referred to as the ground wiring resistance) disposed in the ground wiring 20 extends toward the ground from the node Vf of the f-th circuit 30f on the ground wiring 20. However, since the current source 22 connected to the negative power supply is connected to the ground wiring 20 here, the direction of the current flowing through each ground wiring resistance extends to the current source 22 from the ground.

Accordingly, the voltage drop is also generated on the ground wiring 20 side. Concretely, assuming that the current flowing through a ground wiring resistance Rg1 is Ig1, and the current flowing through a ground wiring resistance Rg2 is Ig2, the voltage drop of a node G1 of the first circuit on the ground wiring 20 from the ground is Rg1×Ig1, and the voltage drop to a node G2 of the second circuit from the node G1 is Rg2×Ig2. Therefore, the voltage drop to the node G2 from the ground is Rg1×Ig1+Rg2×Ig2 which is obtained by integrating the respective voltage drops. Similarly, the voltage drop to the node Gf from the ground indicates a value obtained by integrating all the voltage drops in the respective ground wiring resistances.

Therefore, all the potentials of the respective nodes G1, G2, ... Gf on the ground wiring 20 are lower than a ground potential of 0 V, and drop, as the nodes are

distant from the ground.

As described above, when the current source 22 connected to the negative power supply is not disposed, the direction of the current flowing through the ground wiring 20 extends to the ground from the node Gf. Therefore, as the node on the ground wiring 20 is distant from the ground (in order of G1, G2, ... Gf), the potential of the node increases, and becomes highest in the node Gf. As the node on the ground wiring 18 is distant from the power supply (in order of V1, V2, ... Vf), the potential of the node decreases. As the disposed position of the circuit is distant from the power supply (ground), the potential difference between the node on the power supply side and the node on the ground side in the respective circuits 301 to 30f decreases. Especially, the voltage level in the f-th circuit 30f disposed farthest from the power supply largely drops as compared with the first circuit 301 disposed in the vicinity of the power supply (ground).

On the other hand, in the present embodiment, since the current source 22 connected to the negative power supply is disposed, the direction of the current flowing through the ground wiring 20 extends to the node Gf from the ground. As the node on the ground wiring 20 is distant from the ground (in order of G1, G2, ... Gf), the potential of the node lowers, and becomes lowest in the node Gf. As the node on the ground wiring 18 is distant from the ground (in order of V1, V2, ... Vf), the potential of the node

lowers. Therefore, a sufficient potential difference can be secured between the node on the power supply side and the node on the ground side in the respective circuits 301 to 30f, and the voltage level does not drop even in the circuit disposed in a position distant from the power supply (ground). The circuit is stabilized to such an extent that the circuit is not influenced by the power voltage drop or the ground voltage rise.

It is to be noted that an example in which the negative power supply is disposed outside the semiconductor integrated circuit device has been described in the present embodiment, but the negative power supply may also be built in the semiconductor integrated circuit device.

Moreover, in the present embodiment, the semiconductor integrated circuit device in which the current source is built has been described as an example, but the current source may also be disposed outside the semiconductor integrated circuit device.

[Second Embodiment]

In the first embodiment, the example in which the current source 22 is disposed as the current generating section in the semiconductor integrated circuit device 10 has been described. In a second embodiment, an example in which an operating circuit actually consuming the current to operate is disposed instead of the current source 22 will be described. It is to be noted that a constitution similar to that of the first embodiment is denoted with the

same reference numerals, and the description thereof is omitted.

FIG. 2 is a circuit constitution diagram of a semiconductor integrated circuit device 10a according to the present embodiment.

As shown, an operating circuit is disposed as the current generating section between the node Gf on the ground wiring 20 side and the negative power terminal 16 of the f-th circuit 30f disposed in the region most distant from the ground among a plurality of circuits. It is to be noted that the operating circuit disposed as the current generating section is preferably constituted of a circuit which consumes much current, and a clock generator 24 is used here. After a signal level of an output signal generated by the clock generator 24 is adjusted by a level shifter 26, the signal is outputted to the respective circuits 301 to 30f disposed between the power supply and the ground, and is used as a synchronous signal or the like in the circuits 301 to 30f.

In the present embodiment, since the clock generator 24 connected to the negative power supply is connected to the ground wiring 20, the direction of the current flowing through each ground wiring resistance extends toward the clock generator 24 from the ground. Therefore, in the same manner as in the first embodiment, as the node on the ground wiring 20 is distant from the ground (in order of G1, G2, ... Gf), the potential of the

node lowers. As the node on the ground wiring 18 is distant from the power source (in order of V1, V2, ... Vf), the potential of the node lowers. Therefore, the sufficient potential difference can be secured between the node on the power supply side and the node on the ground side in the respective circuits 301 to 30f, and the voltage level does not drop even in the circuit disposed in the position distant from the power supply (ground). The circuit is stabilized to such an extent that the circuit is not influenced by the power voltage drop or the ground voltage rise.

Moreover, in the present embodiment, since the current flowing toward the negative power supply from the ground is also used for the circuit operation of the clock generator 24, a current supply amount in the whole circuit may be reduced. Furthermore, since the clock generator 24 is disposed as the current generating section, a layout area can be reduced as compared with a case where the current source 22 is disposed.

It is to be noted that an example in which the negative power supply is disposed outside the semiconductor integrated circuit device has been described in the present embodiment, but the negative power supply may also be built in the semiconductor integrated circuit device.

Moreover, in the present embodiment, the semiconductor integrated circuit device in which the operating circuit (clock generator) is built has been

described as the example, but the operating circuit may also be disposed outside the semiconductor integrated circuit device.

It is to be noted that the present invention is not limited to the semiconductor integrated circuit device described as the example in the first and second embodiments, and can be applied to various semiconductor integrated circuit devices.